NeuroMem – powered hardware designs

TRAINABLE NEURAL NETWORK,

K-NN AND RBF CLASSIFIER,

PARALLEL ARCHITECTURE, LOW POWER, SCALABLE

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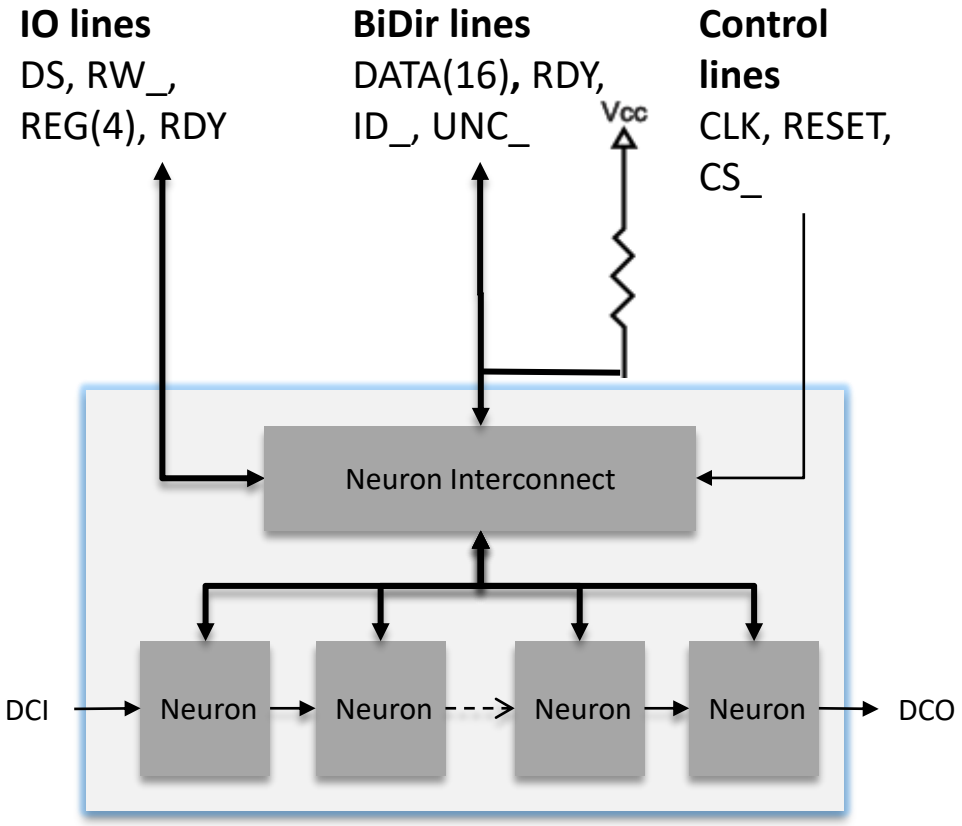
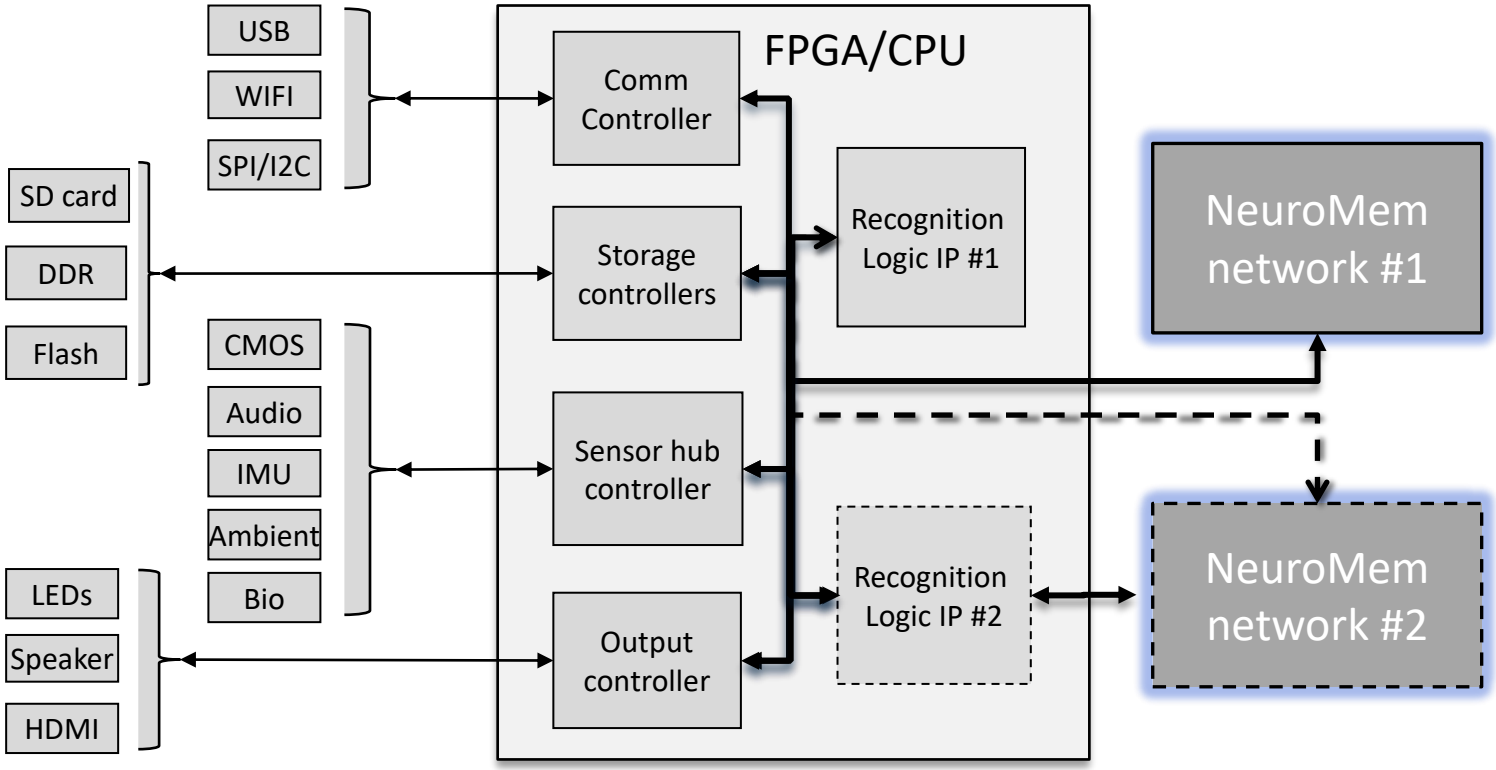
NeuroMem-Bus Interconnect

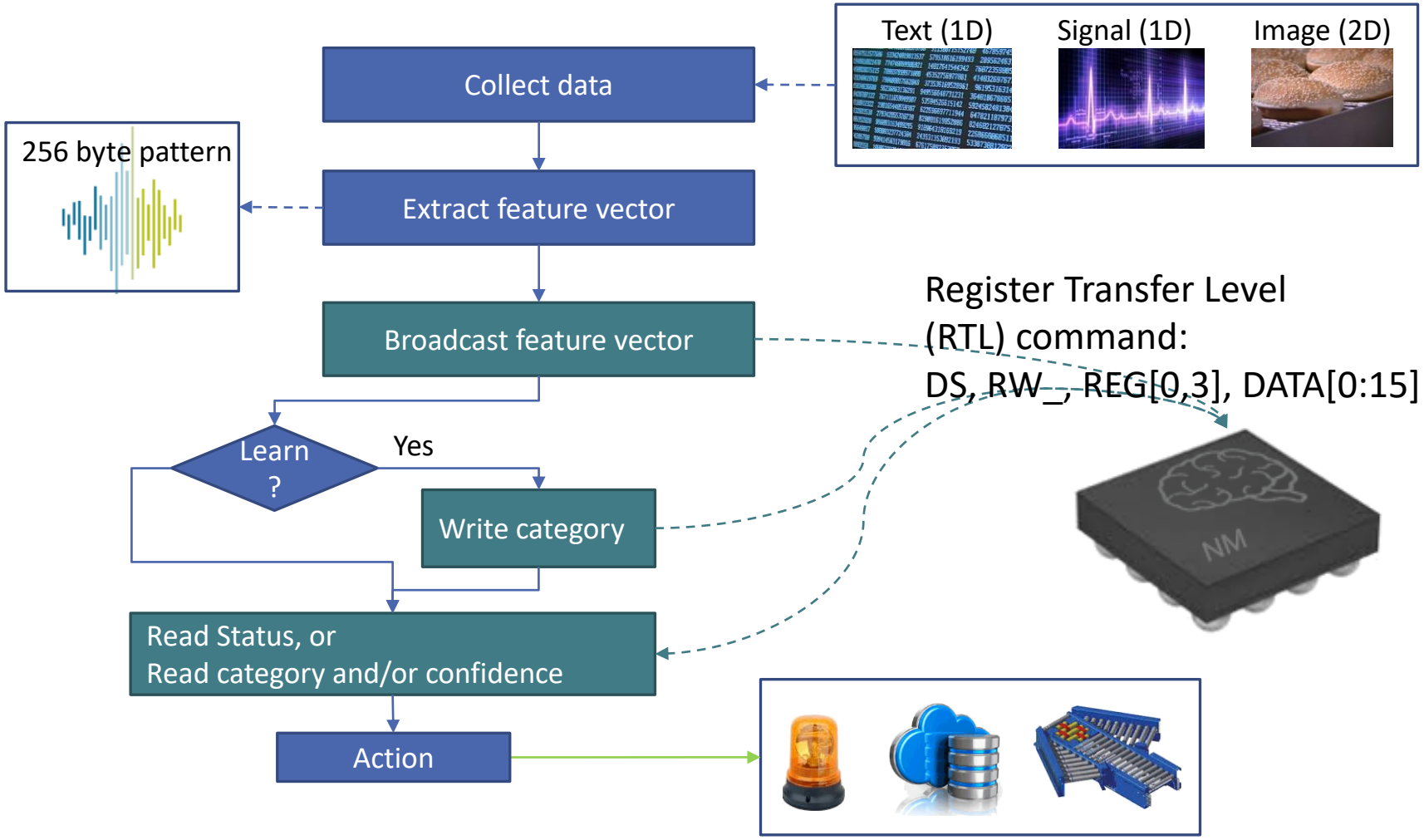
- Identical interconnect between neurons Intra & Inter chips
- 3 control lines
- 7 IO lines
- 19 bidir lines (pulled-up)
- 1 daisy chain line (DCI-DCO)



Classical NM-powered Architecture



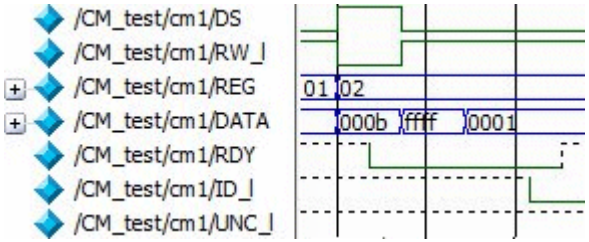
Simple interface



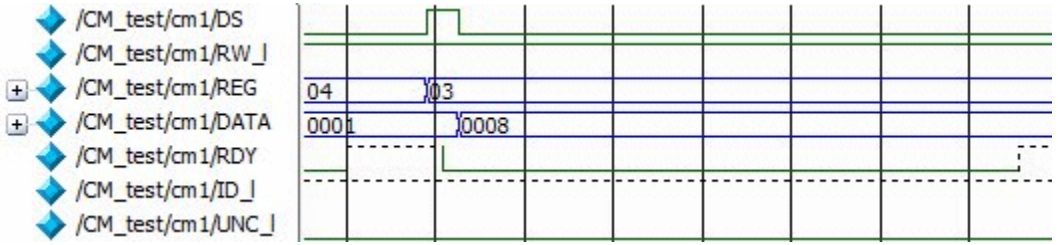
Accessing the neurons

- RTL Commands broadcasted to the NeuroMem bus are sampled on the positive edge of DS by all neurons with Chip_Select (CS_ low)
- Neurons may take different numbers of clock cycles to execute a same command based on their status and content
- The RDY line is pulled down during the execution of the command until all neurons are finished
- Output value can be latched from DATA lines at the rise of RDY

Example of a Write LCOMP (Reg =2) with value 0x000B

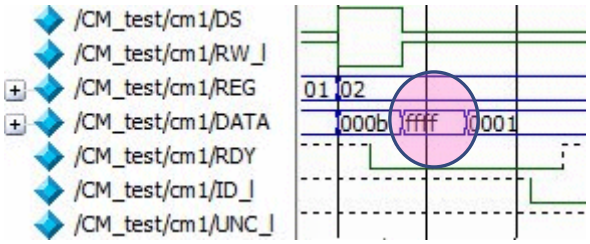


Example of a Read DIST (Reg =3) returning a value0x0008

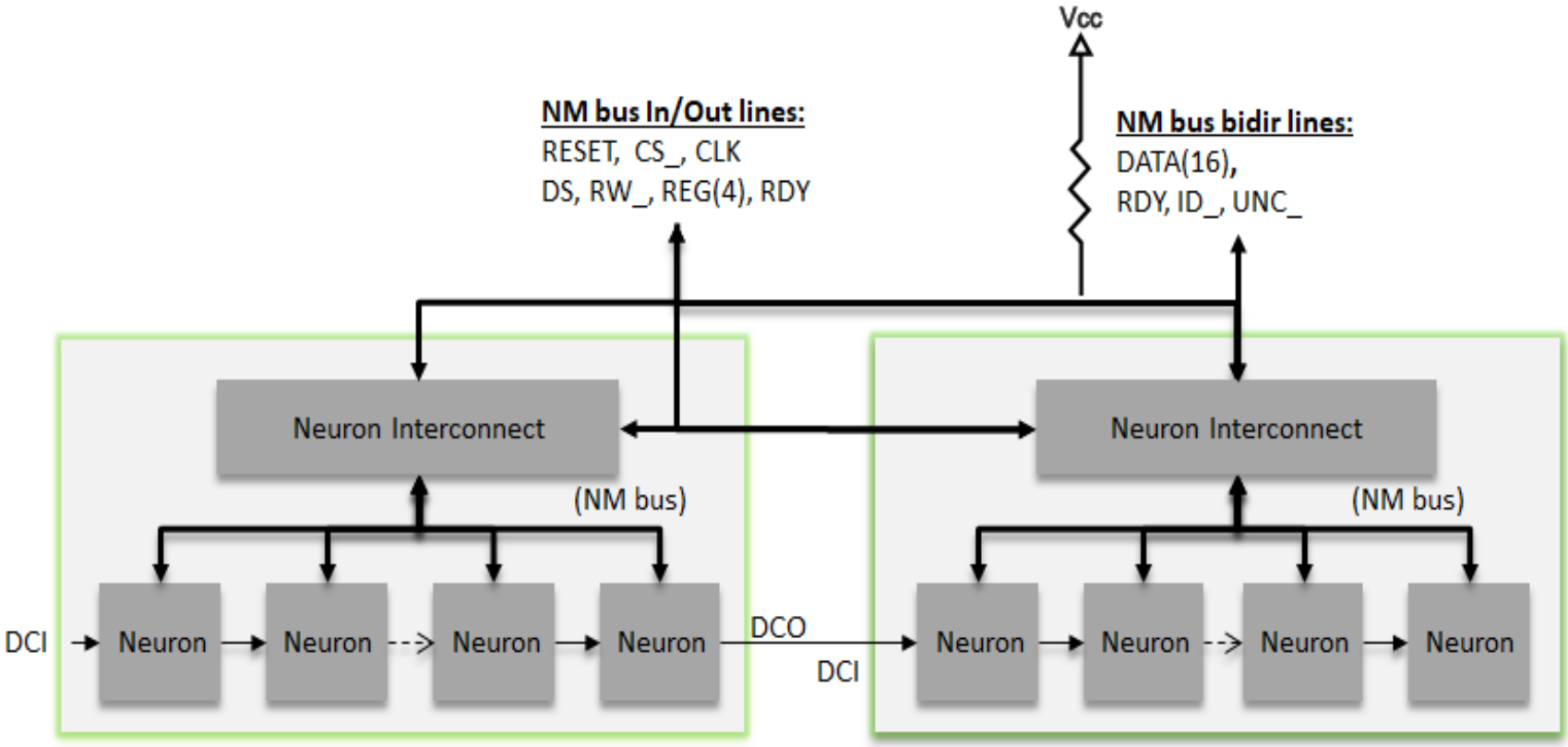


Facts

- Commands take between 1 to 18 clock cycles
- DATA lines default status must be 0xFFFF to ensure that the pull-up resistors are not pulled down and consuming power
- DATA lines must be released (0xFFFF) at the 2nd positive edge of CLK after the rise of DS to enable the interconnectivity between neurons



Multi-chip design

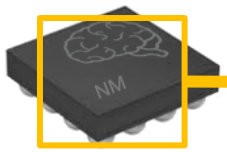


High scalability

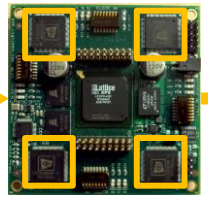
Fixed NeuroMem-bus width regardless of the number of daisy-chained chips

Example of the unique NeuroStack, stackable board

- Hardware
- Firmware

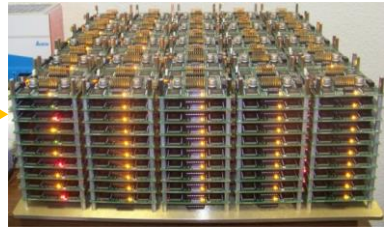


NeuroMem CM1K chip
1024 neurons



1 NeuroStack
4096 neurons

*10 **NeuroStacks***
40960 neurons



1 Million neurons